

DAC8560 Evaluation Module

This user's guide describes the characteristics, operation, and the use of the DAC8560 evaluation module (EVM). It covers all pertinent areas to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

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1 EVM Overview

This section gives a general overview of the DAC8560 evaluation module (EVM), and describes some of the factors to consider when using this module.

1.1 Features

This EVM features the DAC8560 digital-to-analog converter (DAC). The DAC8560 EVM is a simple evaluation module designed to quickly and easily evaluate the functionality and performance of the 16-bit high-resolution, single-channel, and serial input DAC with a built-in 2.5-V internal reference that is enabled by default. This EVM features a serial interface to communicate with any host microprocessor or TI DSP base system.

Although the DAC was designed for single-supply operation, a bipolar output range is also possible by configuring the output operational amplifier circuit properly. This is discussed in detail in section 3.2.3. In addition, the external operational amplifier is also installed as an option to provide output signal conditioning or boost capacitive load drive and for other output mode requirements desired.

A +5-V precision voltage reference is provided via U3 as well as a 4.096-V precision reference via U4. These references are optional voltage reference provided externally in case the user needs to evaluate the DAC8560 with external reference circuits. The external +5-V and +4-V reference source can be selected via W8 and W4 jumper configuration.

There is also a provision for possibly experimenting with different circuit loads on the reference of the DAC8560. These are available through R16, C6, and a small 4x4 through-hole grid.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The DC power supply requirement for this DAC8560EVM (VDD) is selectable between +3.3 V and +5 V via the W1 jumper header. The +3.3 V comes from J6-8 and the +5 V comes from J6-3 terminal, when plugged in via the 5-6k interface board or the HPA449. These power supply voltages are referenced to ground through the J6-6 terminal. The VSS and VCC are only used by the U2 operational amplifier and the U3 voltage reference, which ranges from -15 V to +15 V maximum and connects through J6-1 and J6-2 terminals, respectively. All the analog power supplies are referenced to analog ground through J6-6 terminal.

CAUTION

To avoid potential damage to the EVM board, ensure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses greater than the maximum listed voltage ratings may cause permanent damage to the device.

The negative rail of the output operational amplifier, U2, can be selected between VSS and AGND via the W5 jumper. The external operational amplifier is installed as an option to provide output signal conditioning or for other desired output mode requirements.

CAUTION

To avoid potential damage to the EVM board, ensure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses greater than the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The DAC8560 comes with a +2.5-V internal reference that is enabled by default. The +2.5-V internal reference can be measured from its V_{REF} pin, which can be used to source other devices that requires +2.5-V reference. Because the DAC8560's internal reference is enabled by default, care should be taken to ensure that the W4 and W8 jumper headers are open. Otherwise, inaccurate performance or damage to the part can result. However, the DAC8560 should not be damaged, providing that the external voltage that is applied to the V_{REF} pin does not exceed the applied voltage in the V_{DD} pin, and it does not exceed 100 mA of sourcing current. It is not recommended to leave the external voltage applied on the V_{REF} pin if the internal reference is not disabled. The external reference source should be disconnected immediately, and the EVM power must be recycled to ensure correct performance of the device.

The +5-V and +4-V precision voltage references are provided as an optional reference source to supply the external voltage reference for the DAC through REF02 (U3) and REF3240 (U4). These reference voltages are selectable via the jumper W8. When shorting pins 1 and 2, the +5-V reference is selected whereas shorting pins 2 and 3 selects +4-V reference. The jumper W4 must be shorted between pins 1 and 2 in order for these reference sources to propagate through the DAC.

The +5-V reference voltage goes through an adjustable 100-k Ω potentiometer, R11, in series with 20-k Ω R10, to allow the user to adjust the reference voltage to its desired settings. The voltage reference then is buffered through U5 as seen by the device under test. The REF02 precision reference is powered by V_{CC} (+15 V) through J6-1 terminal.

The REF3240 precision reference is powered by +5 VA through J6-3 terminal.

The test point TP1 also is provided, as well as J4-20, to allow the user to connect other external reference source if the onboard reference circuit is not desired. The external voltage reference should not exceed the applied power supply, V_{DD} , of the DAC under test.

CAUTION

When applying an external voltage reference through TP1 or J4-20, ensure that it does not exceed the applied V_{DD} . Otherwise, this can permanently damage the DAC8560, U1, device under test.

1.3 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8560 digital-to-analog converter (DAC). Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, TI DSP, or some sort of a signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are pass-through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8560 EVM using a custom-built cable.

An adapter interface board (5-6k adapter interface) also is available to fit and mate with TI's C5000™ and C6000™ DSP Starter Kit (DSK). This alleviates the troubles involved in building a custom cable. In addition, this EVM can connect to and interface with an MSP430-based platform (HPA449) that uses the MSP430F449 microprocessor. For more information regarding the 5-6k adapter interface board or the HPA449 platform, call Texas Instruments Incorporated or send an email to dataconvapps@list.ti.com.

The DAC output can be monitored through the selected pins of J4 header connector. The output can be switched through its respective jumper W2 whereas the sense pin V_{FB} also can be switched through its respective jumper W7 for the reason of stacking. The V_{FB} pin is discussed further in section 3 of this user's guide manual. Stacking allows a total of two (DAC8560) DAC channels to be used provided the frame synchronization signal, \overline{SYNC} , is unique for each EVM board stacked.

In addition, the option of selecting the DAC output to be fed to the noninverting side of the output operational amplifier, U2, is also possible by using a jumper across the selected pins of J4. The output operational amplifier, U2, must be first configured correctly for the desired waveform characteristic (see section 3 of this document).

A block diagram of the EVM is shown in [Figure 1](#).

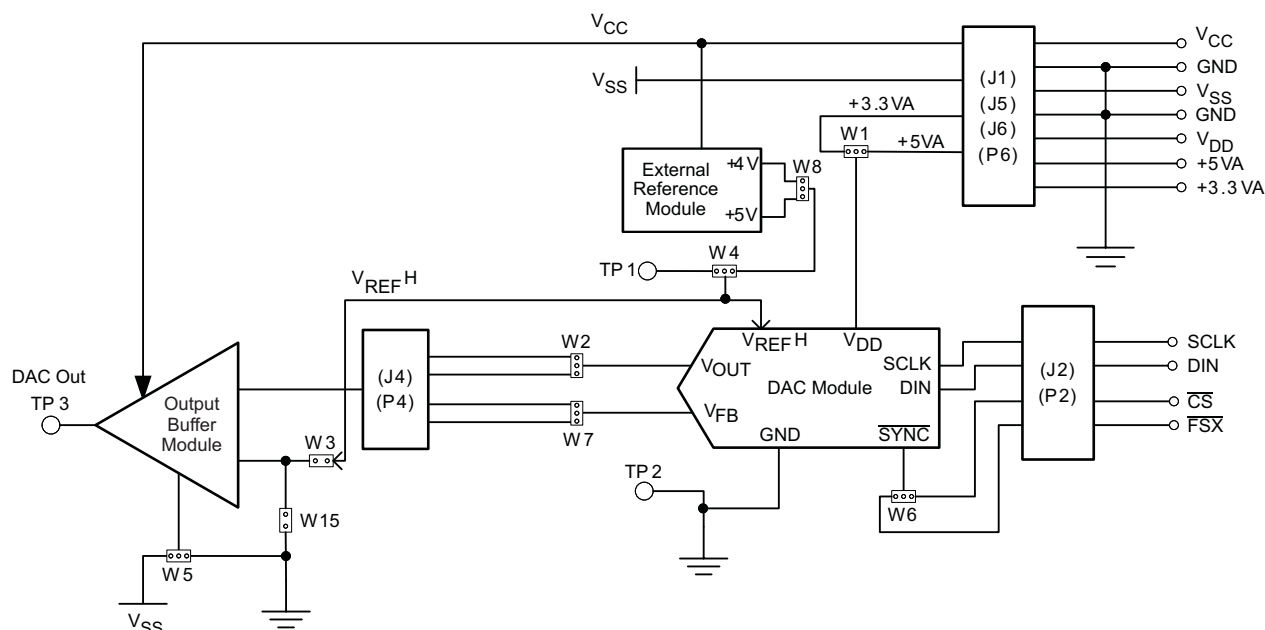


Figure 1. EVM Block Diagram

2 PCB Design and Performance

This section discusses the layout design of the PCB, describes the physical and mechanical characteristics of the EVM, and provides a brief description of the EVM test performance procedure. Also included is the list of components used on this evaluation module.

2.1 PCB Layout

The DAC8560EVM is designed to preserve the performance quality of the DAC, device under test, as specified in the data sheet. To take full advantage of the EVM's capabilities, use care during the schematic design phase to properly select the right components and to build the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals, and understanding the components' electrical and mechanical attributes.

The main design concern during the layout process is the optimal placement of components and the proper routing of signals. Place the bypass capacitors as close as possible to the pins; properly separate the analog and digital signals from each other. In the layout process, carefully consider the power and ground plane because of their importance. A solid plane is ideally preferred, but because of its greater cost, sometimes a split plane can be used satisfactorily. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the DUT. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning that the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practices are illustrated in [Figure 2](#) through [Figure 8](#).

The DAC8560 EVM board is constructed on a four-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2500 inch), and the board thickness is 1,5748 mm (0.062 inch). [Figure 2](#) through [Figure 6](#) show the individual artwork layers.

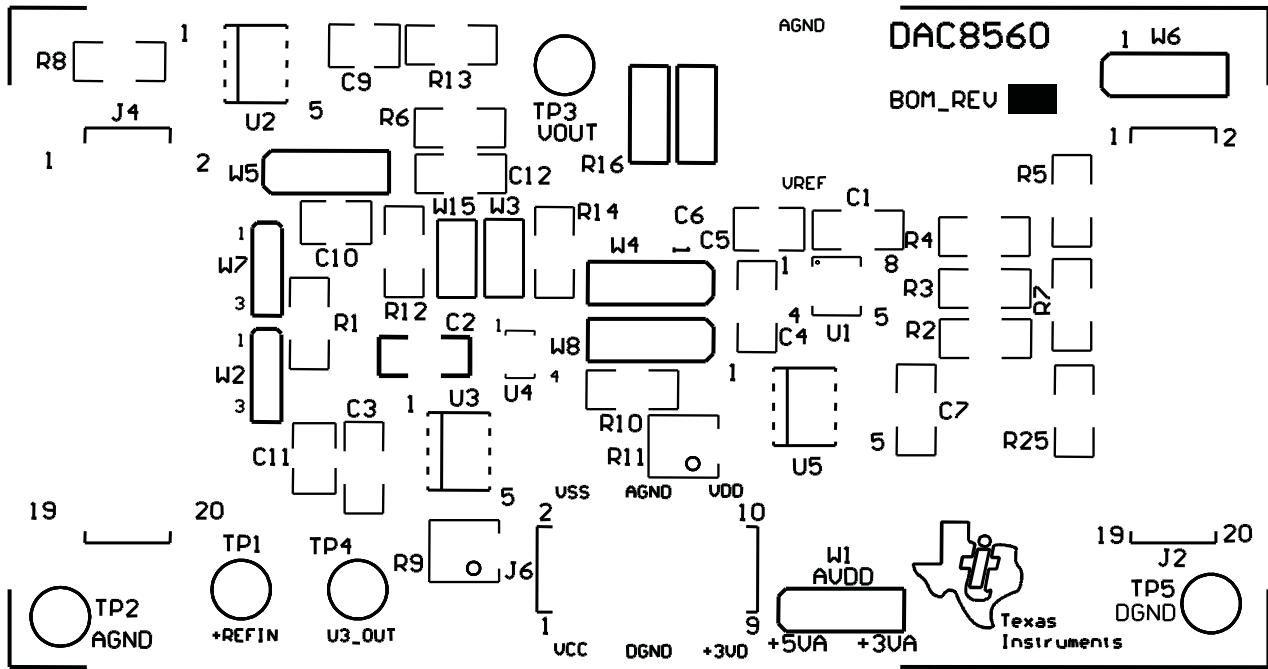


Figure 2. Top Silkscreen

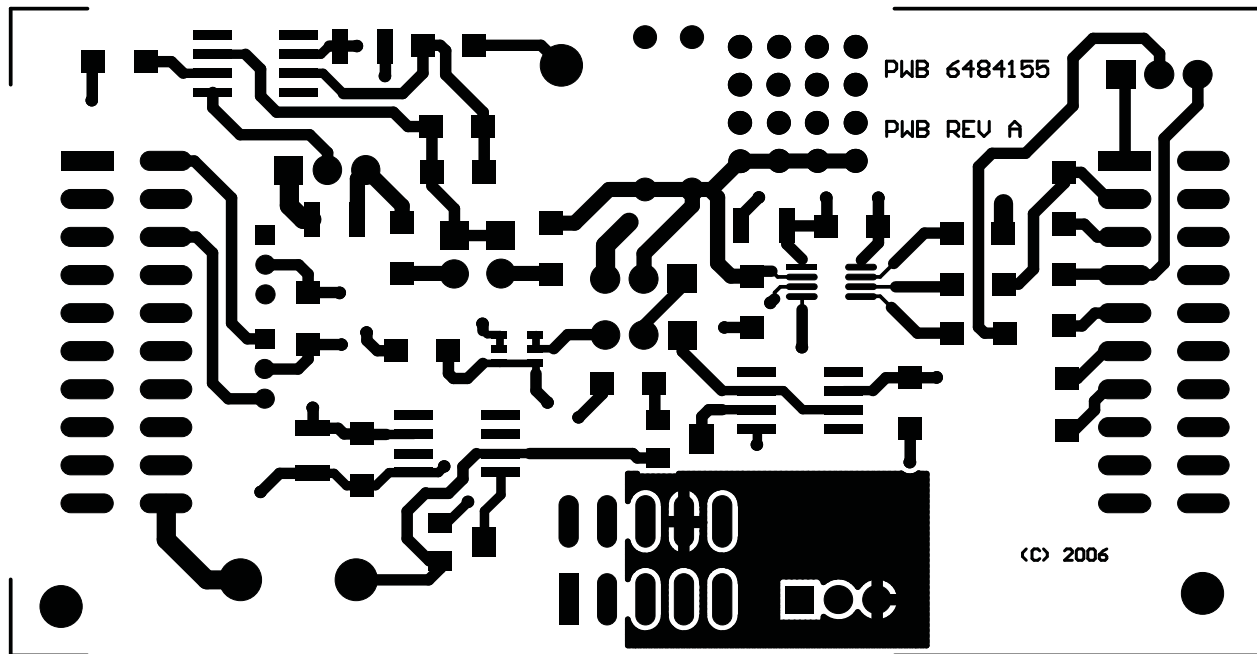


Figure 3. Layer 1 (Top Signal Plane)

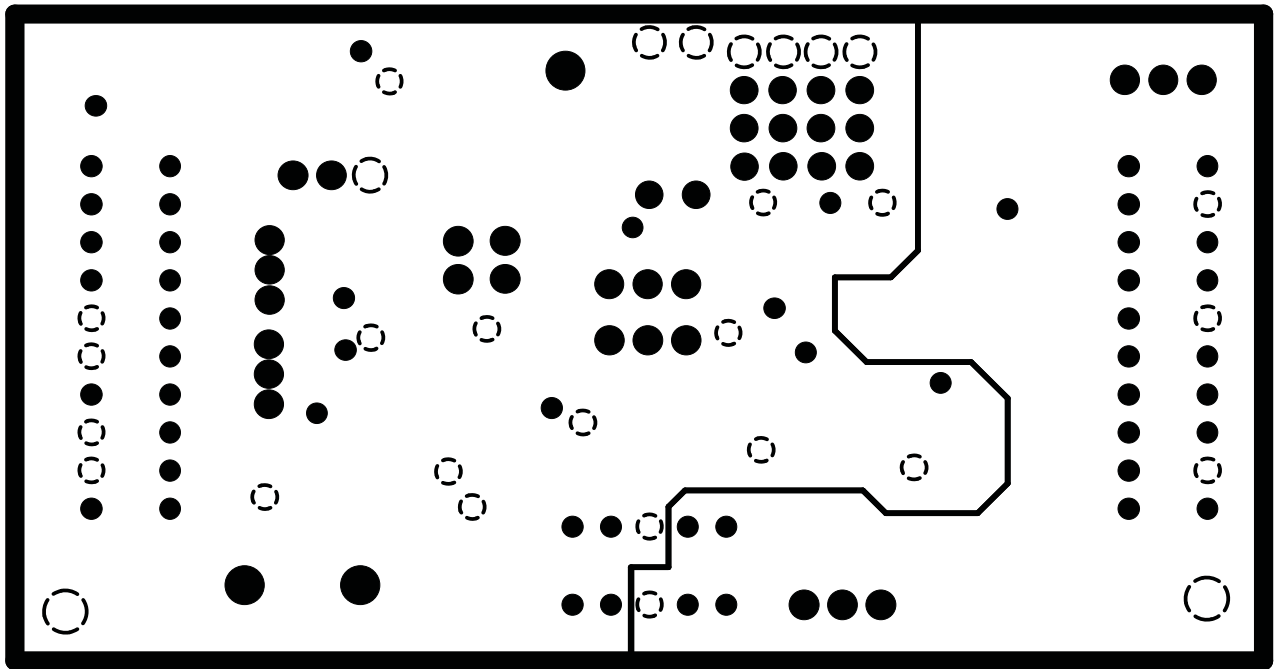


Figure 4. Layer 2 (Ground Plane)

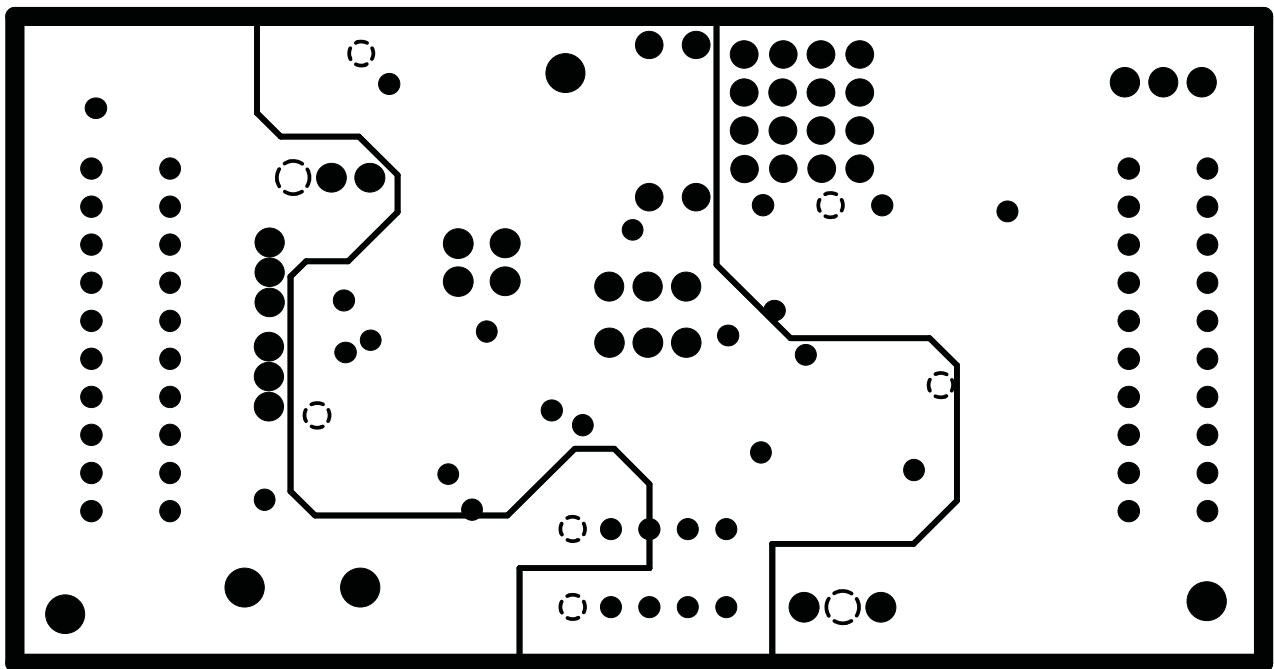


Figure 5. Layer 3 (Power Plane)

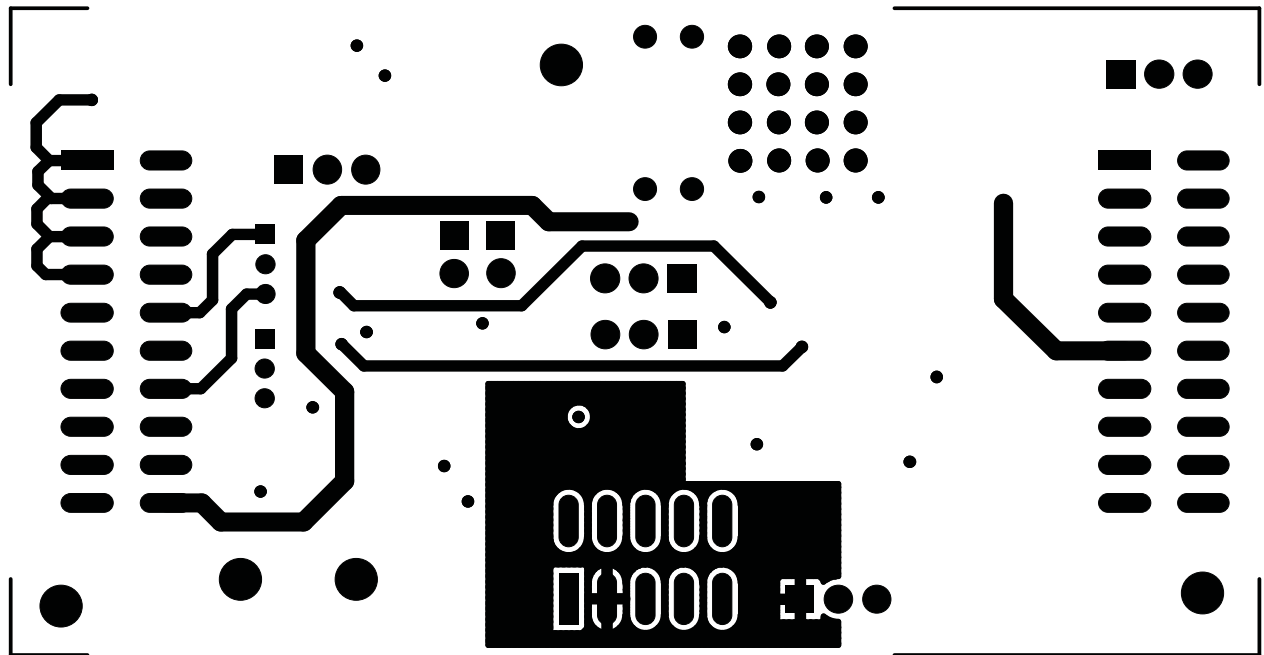


Figure 6. Layer 4 (Bottom Signal Plane)

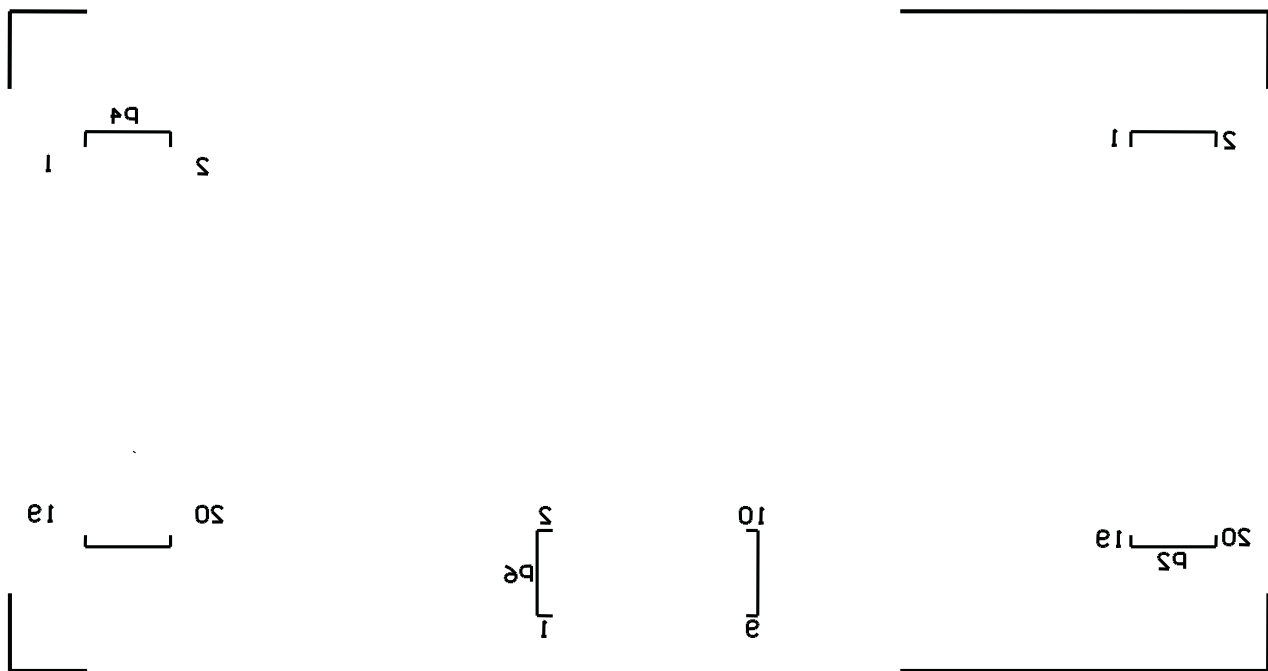
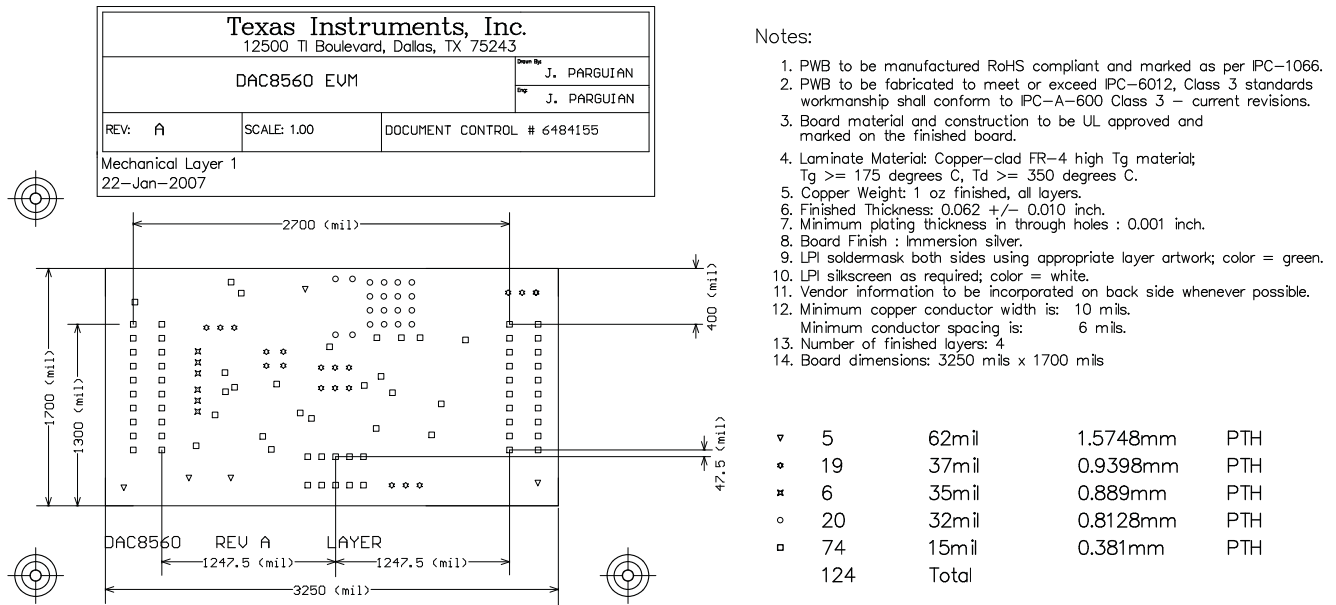


Figure 7. Bottom Silkscreen


Figure 8. Drill Drawing

2.2 EVM Performance

The EVM performance test is performed using a high-density DAC bench test board, an Agilent 3458A digital multimeter, and a PC running the LABVIEW software. The EVM board is tested for all codes of 65535 and the device under test (DUT) is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

Figure 9 shows the INL and DNL characteristic plots.

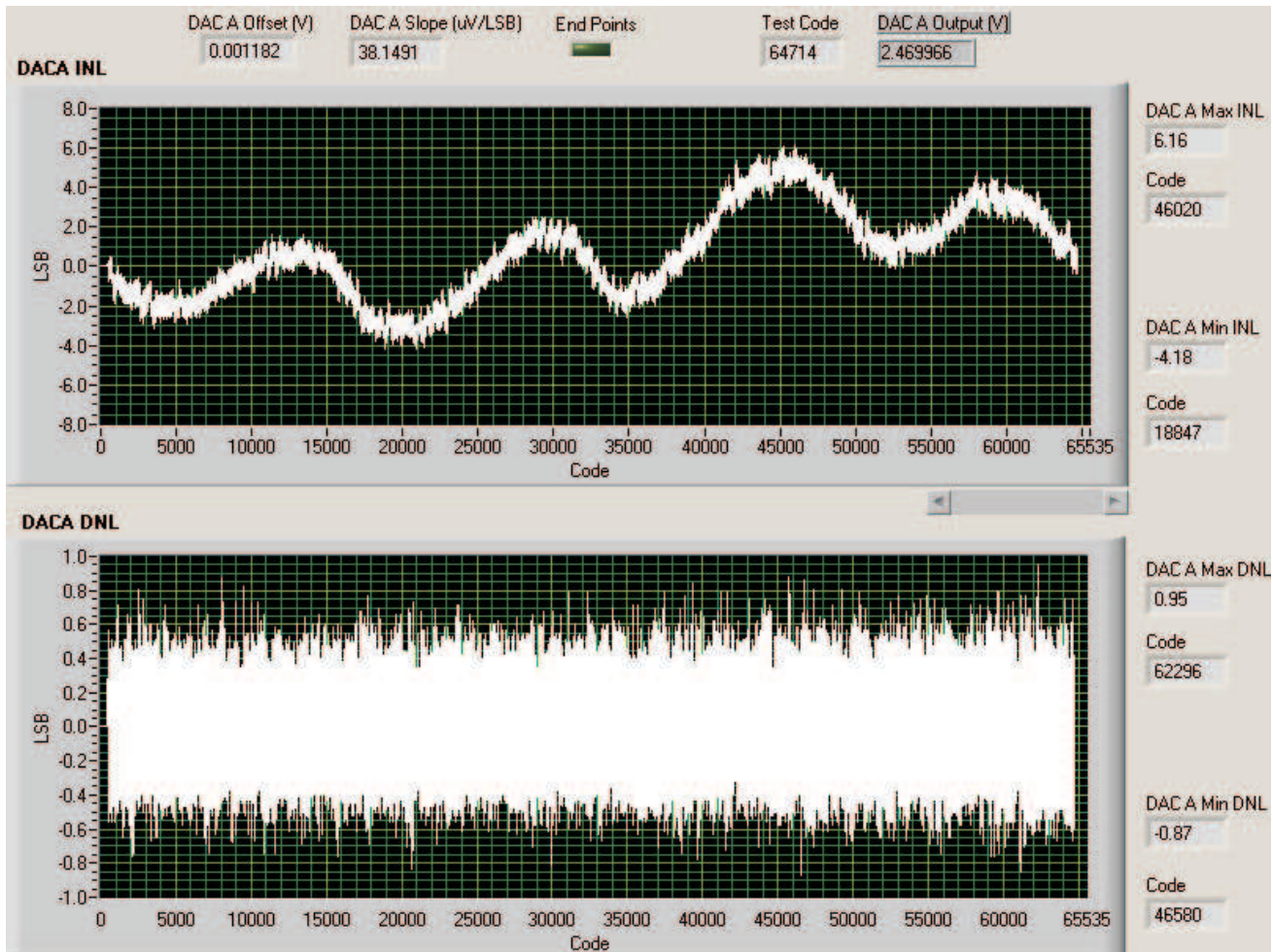


Figure 9. INL and DNL Characteristic Plot

2.3 Bill of Materials

Table 1. Parts Lists

Item	Qty	Value	Designators	Description	Vendor	Vendor Part No.
1	3	10kΩ	R6 R12 R14	1/8W 1206 Thick Film Chip Resistor, ±1% Tol	Panasonic	ERJ-8ENF1002V
2	1	20kΩ Trim Pot	R9	5T Potentiometer, 4mm SMD, Cermet	Bourns	3214W-1-203E
3	5	0 Ω	R1–R4 R8	1/4 W 1206 Thick Film Chip Resistor, ±5% Tol	Panasonic	ERJ-8GEY0R00V
4	1	100 Ω	R13	1/4W 1206 Thick Film Chip Resistor, ±5% Tol	Panasonic	ERJ-8GEYJ101V
5	1	20kΩ	R10	1/4W 1206 Thick Film Chip Resistor, ±5% Tol	Panasonic	ERJ-8GEYJ203V
6	1	100kΩ Trim Pot	R11	Potentiometer, 4mm SMD, Cermet	Bourns	3214W-1-104E
7	3	0.1μF	C1 C3 C7	Multilayer Ceramic Chip Capacitor, 1206 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3216X7R1E104KT
8	2	1μF	C9 C10	Multilayer Ceramic Chip Capacitor, 1210 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3225X7R1E105KT
9	1	1nF	C12	Multilayer Ceramic Chip Capacitor, 1206 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3216X7R1H102KT
10	1	0.47μF	C2	Multilayer Ceramic Chip Capacitor, 1206 SMD, 50V, ±15% TC, ±10% Tol	TDK	C3216X7R1H474KT
11	2	10μF	C5 C11	Multilayer Ceramic Chip Capacitor, 1210 SMD, 25V, ±15% TC, ±10% Tol	TDK	C3225X7R1E106KT

Table 1. Parts Lists (continued)

Item	Qty	Value	Designators	Description	Vendor	Vendor Part No.
12	1	100pF	C4	Multilayer Ceramic Chip Capacitor, 0603 SMD, 50V, 30ppm/°C, ±5% Tol	TDK	C1608COG1H101J
13	1	Bipolar Op-Amp	U5	8-SOP(D) High Precision Low Noise Op-Amp	Texas Instruments	OPA227UA
14	1	16-Bit String DAC	U1	MSOP-8(DGK), 1-CH, SPI, Low Glitch, Voltage Output DAC with Internal reference	Texas Instruments	DAC8560IDDGK
15	1	4.096V Reference	U4	4ppm/°C, 100µA, SOT23-6 VOLTAGE REFERENCE	Texas Instruments	REF3240AIDBV
16	1	5V Reference	U3	15ppm/°C, ±0.2% Tol Output, SOIC-8, Voltage Reference	Texas Instruments	REF02AU
17	1	Difet Op-Amp	U2	8-SOP(D) Precision High-Speed, Difet Op-Amp	Texas Instruments	OPA627AU
18	2	10 × 2 × 0.1 SMT	J2 J4	20-PIN Terminal Strip	Samtec	TSM-110-01-S-DV-M
19	1	5 × 2 × 0.1 SMT	J6	10-PIN Terminal Strip	Samtec	TSM-105-01-T-DV
20	2	10 × 2 × 0.1 SMT	P2 P4	20-PIN Socket Strip ⁽¹⁾	Samtec	SSW-110-22-S-D-VS-P
21	1	5 × 2 × 0.1 SMT		P6 10-PIN Socket Strip ⁽¹⁾	Samtec	SSW-105-22-F-D-VS-K
22	5	1 × 1 × 0.061D TH	TP1–TP5	Turret Terminal Pin	Mill-Max	2348-2-00-01-00-00-07-0
23	2	3 × 1 × 0.7874 TH	W2 W7	3-PIN Terminal Strip	Samtec	TMM-103-01-T-S
24	2	2 × 1 × 0.1 TH	W3 W15	Modified 0.025" Square Post Header	Samtec	MTSW-102-08-T-S-295
25	5	3 × 1 × 0.1 TH	W1 W4–W6 W8	Modified 0.025" Square Post Header	Samtec	MTSW-103-08-T-S-295
26	0	N/A	N/A	Schematic Diagram	Texas Instruments	6484156
27	1	N/A	N/A	Printed Wiring Board	Texas Instruments	6484155
28	0	N/A	N/A	Printed Circuit Assembly	Texas Instruments	6484157
29	0	N/A	N/A	29 0 N/A N/A Kit Assembly	Texas Instruments	6484158
30	5	Do Not Populate	C6 R5 R7 R16 R25	Do not install these components ⁽¹⁾		
31	1	2mm Shunt	N/A	Shorting Block for W2	Samtec	2SN-BK-G
32	6	0.100 Shorting Blocks	N/A	Shorting Blocks	Samtec	SNT-100-BK-G-H

⁽¹⁾ P2, P4, and P6 parts are not shown in the schematic diagram. All the P-designated parts are installed in the bottom side of the PC board opposite the J-designated counterpart. Example, J2 is installed on the topside whereas P2 is installed in the bottom side opposite of J2. **Do NOT** install the following: C6, R5, R7, R16, and R25.

3 EVM Operation

This section covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

See the DAC8560 data sheet, ([SBAS254](#)), for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in the unipolar output mode.

3.1 Factory Default Setting

The EVM board is set to its default configuration from factory as described in [Table 2](#) to operate in unipolar +2.5-V mode of operation. [Figure 10](#) shows the default jumper configuration as described in the table for the DAC8560.

Table 2. Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	1-2	Analog supply for the DAC8560 is +5 VA.
W2	1-2	DAC output (V_{OUT}) is routed to J4-2.
W3	OPEN	V_{REF} is not routed to the inverting input of the operational amplifier for voltage offset (for bipolar mode of operation).
W4	OPEN	Onboard external buffered reference U3 or U4 is not routed to V_{REF} .
W5	1-2	Negative supply rail of U2 operational amplifier is supplied with V_{SS} .
W6	1-2	\overline{CS} signal from J2 is used for frame synchronization, \overline{SYNC} , signal.
W7	OPEN	For DAC8560 EVM, the V_{FB} is not routed out unless there is a need to minimize the output error. If using W7, remove R1 and short W7, then connect V_{FB} and V_{OUT} as close as possible to the load.
W8	OPEN	Onboard external buffered reference U3 or U4 are not selected. Default is the +2.5-V internal reference of the DAC8560.
W15	OPEN	Output operational amplifier, U2, is configured as voltage follower.
J4	1-2	DAC output (V_{OUT}) is connected to the noninverting input of the output operational amplifier, U2.

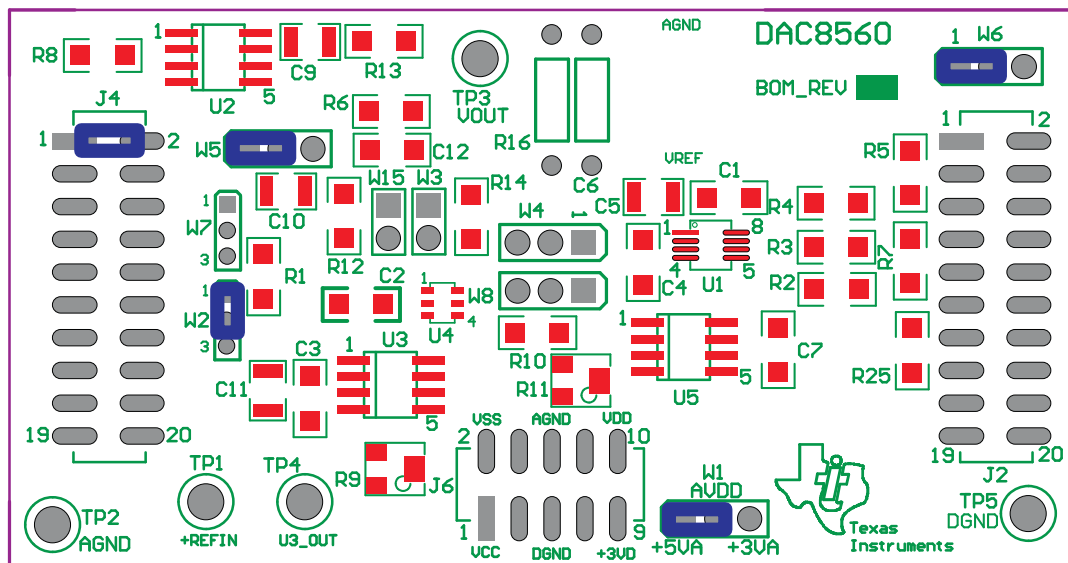


Figure 10. DAC8560 EVM Default Jumper Configuration

3.2 Host Processor Interface

The host processor basically drives the DAC; so, the DAC's proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code also is required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

An interface adapter board also is available for a specific TI DSP starter kit as well as an MSP430-based microprocessor as previously mentioned. Using the interface board alleviates the tedious task of building customized cables and allows easy configuration of a simple evaluation system.

The DAC8560 interfaces with any host processor capable of handling SPI protocols or the popular TI DSP. For more information regarding the DAC8560 data interface, see the DAC8560 data sheet ([SLAS464](#)).

3.3 EVM Stacking

The stacking of EVMs is possible if the user needs to evaluate two DAC8560 devices to yield a total of up to two (DAC8560) channel outputs. A maximum of two EVMs are allowed because the output terminal, J4, dictates the number of DAC channels that can be connected without output bus contention. [Table 3](#) shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper position of W2 and W7.

Table 3. DAC Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	DAC output (V_{OUT}) is routed to J4-2.
	2-3	DAC output (V_{OUT}) is routed to J4-6.
W7	1-2	DAC sense pin (V_{FB}) is routed to J4-10, if R1 jumper resistor is disconnected.
	2-3	DAC sense pin (V_{FB}) is routed to J4-14, if R1 jumper resistor is disconnected.

In order to allow exclusive control of each EVM that is stacked together, the DAC8560 must have a separate \overline{SYNC} signal. This is accomplished in hardware by routing the \overline{SYNC} signal of the first EVM through \overline{CS} (P2/J2 pin 1) by shorting pins 1-2 of jumper W6. The second EVM should use the \overline{FSX} signal (P2/J2 pin 7) to drive the \overline{SYNC} signal by shorting pins 2-3 of the jumper W6. The output can be mapped as described in [Table 3](#) for each of the EVM stacked.

3.4 The Output Operational Amplifier

The EVM includes an optional signal-conditioning circuit for the DAC output through an external operational amplifier, U2. During stacking of the EVMs, only one DAC output channel can be monitored at any given time for evaluation because the odd-numbered pins (J4-1 to J4-7) are tied together. If both outputs are needed to be buffered and monitored at the same time, the traces in the back of the EVM board are exposed for ease of cutting. When cutting a trace, make sure to cut through the trace adjacent to the appropriate J4 header pin and not at the curvy line. If the trace is cut through the curving line, the signal may not propagate through to the operational amplifier. See [Figure 6](#) and the schematic included in this manual.

The output operational amplifier is set to unity gain configuration by default but can be modified by simple jumper settings. Nevertheless, the raw output of the DAC can be probed through the specified pins of the J4 output terminal, which also provides mechanical stability when stacking or plugging into any interface board. In addition, it provides easy access for monitoring up to two (DAC8560) DAC channels when stacking two EVMs together (see section 3.3).

The following sections describe the different configurations of the output amplifier, U2.

3.4.1 Unity Gain Output

The buffered output configuration can be used to prevent loading the DAC8560, although it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match the desired wave shape by simply desoldering R6 and C12 and replacing them with components of the desired values. You can also simply eliminate R6 and C12 altogether and just solder a 0- Ω resistor in replacement of R6, if desired.

[Table 4](#) shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

Table 4. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Open	Open	Disconnect V_{REF} from the inverting input of the operational amplifier.
W5	2-3	1-2	Supplies V_{SS} to the negative rail of operational amplifier or ties it to AGND.

Table 4. Unity Gain Output Jumper Settings (continued)

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W15	Open	Open	Disconnect the negative input of the operational amplifier from the gain resistor, R12.

3.4.2 Output Gain of Two or Bipolar Operation

Two types of configurations yield a gain of two output, depending on the setup of the jumpers W3 and W15. These configurations allow the user to choose a DAC output having V_{REF} as an offset or not.

Table 5 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

Table 5. Gain of Two Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Close	Close	Inverting input of the output operational amplifier, U2, is connected to V_{REF} for use as its offset voltage for bipolar operation. W15 jumper must be open.
	Open	Open	V_{REF} is disconnected from the inverting input of the output operational amplifier, U2. W15 jumper must be close to achieve gain of 2 output.
W5	2-3	1-2	Supplies power, V_{SS} , to the negative rail of operational amplifier, U2, for bipolar mode, or ties it to AGND for unipolar mode.
W15	Close	Close	Configures operational amplifier, U2, for a gain of 2 output without a voltage offset. W3 jumper must be open.
	Open	Open	Inverting input of the operational amplifier, U2, is disconnected from the gain resistor, R12. W3 jumper must be close.

3.4.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirement. However, all operational amplifiers under certain conditions may become unstable depending on the operational amplifier configuration, gain, and load value. These are just few factors that can affect operational amplifiers stability performance and should be considered when implementing.

In unity gain, the OPA627 operational amplifier, U2, performs well with large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and by adding a load resistor even improves the capacitive load drive capability.

Table 6 shows the jumper setting configuration for a capacitive load drive.

Table 6. Capacitive Load Drive Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Open	Open	V_{REF} is disconnected from the inverting input of the output operational amplifier, U2.
W5	2-3	1-2	Supplies power, V_{SS} , to the negative rail of operational amplifier, U2, for bipolar mode, or ties it to AGND for unipolar mode.
W15	Open	Open	Capacitive load drive output of DAC is routed to pin 1 of W15 jumper and can be used as the output terminal.

3.5 Jumper Setting

Table 7 shows the function of each specific jumper setting of the EVM.

Table 7. Jumper Setting Function























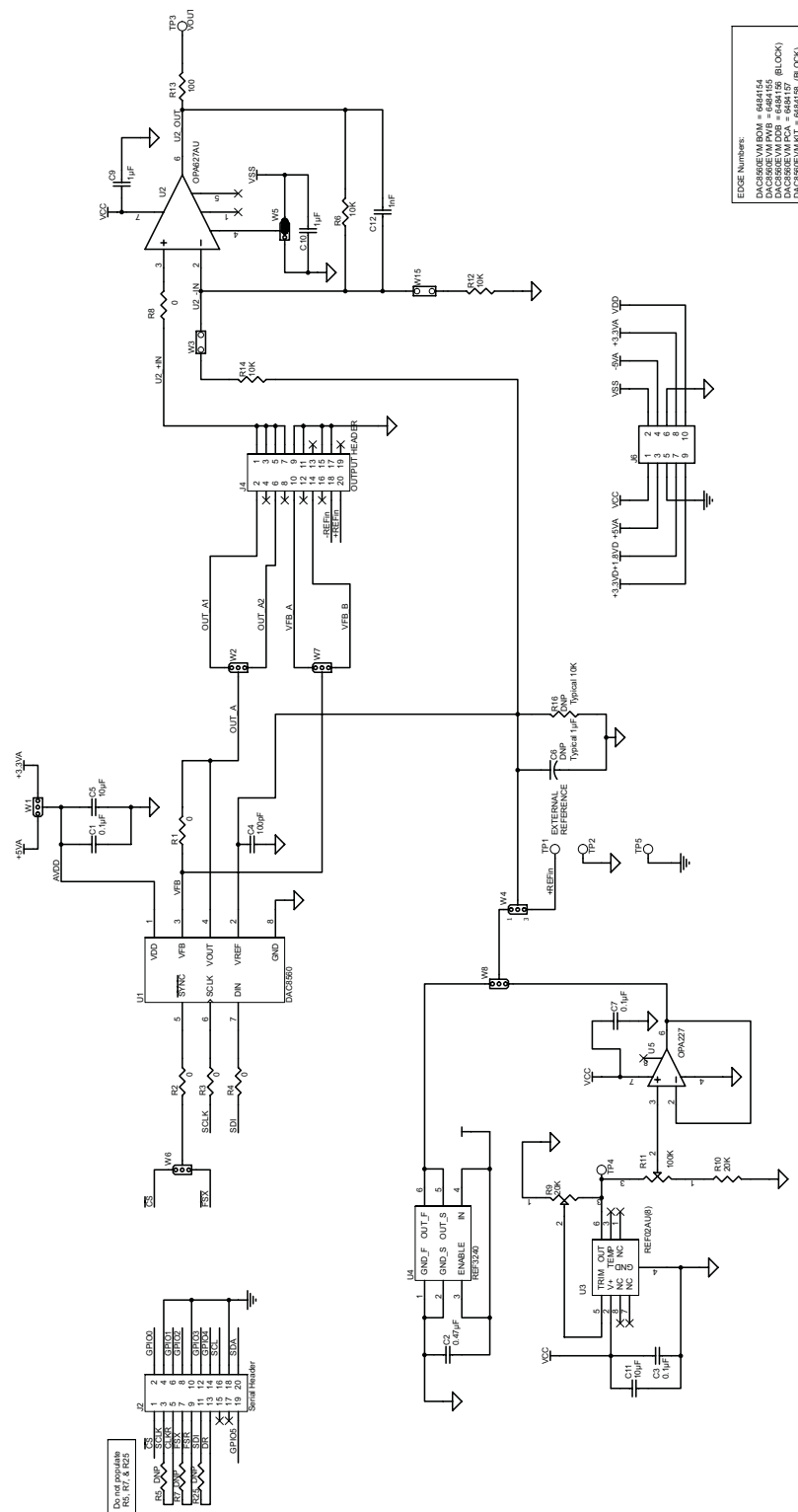
Reference	Jumper Position	Function
W1		+5-V analog supply is selected for AV_{DD} .
		+3.3-V analog supply is selected for AV_{DD} .
W2		Routes V_{OUT} to J4-2.
		Routes V_{OUT} to J4-6.
W3		Disconnects V_{REF} to the inverting input of the output operational amplifier, U2
		Connects V_{REF} to the inverting input of the output operational amplifier, U2
W4		Routes the adjustable, onboard +5-V reference or the fixed +4-V reference to the V_{REF} input of the DAC8560.
		This is the default jumper position for DAC8560 EVM because the +2.5-V internal reference is enabled by default.
		Routes the user-supplied reference from TP1 or J4-20 to the V_{REF} input of the DAC8560.
W5		Negative supply rail of the output operational amplifier, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output operational amplifier, U2, is tied to AGND for unipolar operation.
W6		\overline{CS} signal from J2-1 is routed to drive the \overline{SYNC} signal of the DAC8560.
		\overline{FSX} signal from J2-7 is routed to drive the \overline{SYNC} signal of the DAC8560.
W7		For DAC8560 EVM, the V_{FB} is routed out to minimize the output error. Remove R1 and short W7 as shown; then connect V_{FB} and V_{OUT} as close as possible to the load. The V_{FB} signal will be routed to J4-10.
		This is the default jumper position for DAC8560 EVM when R1 is installed.
		For DAC8560 EVM, the V_{FB} is routed out to minimize the output error. Remove R1 and short W7 as shown then connect V_{FB} and V_{OUT} as close as possible to the load. The V_{FB} signal will be routed to J4-14.
W8		This jumper position selects the adjustable +5-V reference to route to the V_{REF} input of the DAC8560.
		This is the default jumper position for DAC8560 EVM because the +2.5-V internal reference is enabled by default.
		This jumper position selects the +4-V reference to route to the V_{REF} input of the DAC8560.
W15		Disconnects the inverting input of the output operational amplifier, U2, from the gain resistor, R12.
		Connects the inverting input of the output operational amplifier, U2, to the gain resistor, R12, for gain of 2 configuration.

Table 7. Jumper Setting Function (continued)

Reference	Jumper Position	Function
Legend:  Indicates the corresponding pins that are shorted or closed.		

3.6 Schematics



4 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this manual by its title and literature number. Updated documents also can be obtained through the TI Web site at www.ti.com.

Data Sheet:	Literature Number:
DAC8560	SBAS254
REF02	SBVS003
REF3240	SBVS058
OPA627	SBOS165
OPA227	SBOS110

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It is important to operate this EVM within the input voltage range of +2.7 V to +5 V and the output voltage range of -5 V to +5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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